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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,898	10/22/2003	David Scott Nelson	907A.0138.U1(US)	6357

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EXAMINER	
BENGHUZZI, MOHSIN M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,898	NELSON ET AL.	
	Examiner	Art Unit	
	Mohsin (Ben) Benghuzzi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-21* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *October 22, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 4-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Claim 4 contains the term 'error-formatter,' which was not described in the specification. Based upon the disclosed specification, examiner will, hereinafter, interpret the term to mean a bit splitter.

Claim Objections

3. Claims 4 and 5 are objected to because of the following informalities:

The claims recite the limitation 'fractional interpolator filter' in claim 1. There is insufficient antecedent basis for this limitation in the claim. Examiner suggests removal of 'filter' from the limitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 7, 10, 11, and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller (US Pub 2003/0204542) in view of Gardner et al. (US 5,805,619).

1) Regarding claim 1:

Mueller discloses a circuit for re-sampling N data inputs comprising:

an oscillator having an input coupled to an output of the timing error-detector sub-circuit and N timing signal outputs for outputting N timing signals in parallel and a second output for outputting the strobe (Paragraph 0025 Lines 1-4 and Page 4, Claim 1 Lines 3-4); and

at least one fractional interpolator having parallel inputs coupled to N data inputs in parallel and to the N timing signals in parallel, for outputting N data outputs in parallel, wherein N is an integer greater than or equal to one (Paragraph 0024 Lines 4-7 and Page 4, Claim 1 Line 2).

Mueller does not disclose a timing error detector sub-circuit having a first input coupled to a symbol rate clock and a second input coupled to a strobe. However, Gardner et al. discloses a timing error detector sub-circuit having a first input coupled to

a symbol rate clock and a second input coupled to a strobe (Column 2 Line 59 to Column 3 Line 5).

It is clearly obvious to one of ordinary skill in the art that a timing error detector is desirable in a circuit for re-sampling N data inputs. A timing error detector allows for the measurement of the timing error in a strobe (See Gardner et al., Column 2 Lines 63-66) and that in turn allows for error correction. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a timing error detector in the re-sampling circuit of Mueller, as Gardner et al. teaches, in order to allow for error correction.

2) Regarding claim 7:

Gardner et al. discloses, wherein the error detector sub-circuit operates to synchronize the strobe (Column 2 Lines 63-66 and Column 5 Lines 34-36).

Although Mueller or Gardner et al. do not specifically disclose, wherein the error detector sub-circuit operates to synchronize the strobe to a positive edge of the input that is coupled to the symbol rate clock, such limitation is merely a matter of design choice and would have been obvious in the system of Mueller or Gardner et al. The choice of synchronization of the strobe to a positive or negative edge is dependent upon the type of the input.

3) Regarding claim 10:

Gardner et al. discloses, wherein the error detector sub-circuit synchronizes the strobe by adjusting a period between two consecutive strobes to match a period defined by the symbol rate clock (Column 8 Lines 16-19 and Column 5 Lines 11-13,

wherein, 'aligning the sampling strobe timing' and 'data signal is strobed (sampled) at properly timed intervals T' is interpreted as adjusting a period between two consecutive strobes to match a period defined by the symbol rate clock).

4) Regarding claim 11:

Gardner et al. discloses, wherein the error detector sub-circuit further comprises an oscillator data clock having an input coupled to the strobe, and an integrator having a first input coupled to an output of the oscillator data clock and a second input coupled to an output of the symbol rate clock, the integrator having an output coupled to an inverter, and wherein the oscillator input is coupled to an output of the inverter (Column 2 Lines 63-67 and Column 22 Lines 42-44, wherein, block 371 in Fig. 20 is interpreted as the inverter).

5) Regarding claim 13:

Mueller teaches a method for re-sampling a data sample input at any fractional time within of a symbol period, comprising:

synchronizing a local clock to a symbol clock (Paragraph 0034 Lines 11-13);

determining a timing signal based on the synchronized local clock (Paragraph 0005 Lines 12-13 and Lines 20-22);

providing the timing signal and a strobe to an interpolating filter (Paragraph 0006 Lines 1-9);

providing a timing feedback to synchronize the local clock to the symbol clock (Paragraph 0005 Lines 16-20).

Mueller does not teach, re-sampling a data sample input at a time within a symbol period determined by the timing signal and the strobe. However, as discussed in claim 10 above, Gardner et al. teaches, re-sampling a data sample input at a time within a symbol period determined by the timing signal and the strobe (Column 8 Lines 16-19 and Column 5 Lines 11-13, wherein, 'coincide with the instants of ideal signal levels' is interpreted as the time within a symbol period).

6) Regarding claim 14:

Gardner et al. teaches, wherein synchronizing a local clock to a symbol clock comprises determining a difference between the symbol rate clock signal and one of at least two data strobes and providing a frequency adjustment output based on the difference (Column 8 Lines 16-19 and Column 5 Lines 11-13, wherein, 'output error control signal' is interpreted as providing a frequency adjustment output).

7) Regarding claim 15:

Gardner et al. teaches, wherein the timing feedback comprises a most significant bit of an amplified frequency signal accumulated in a register (Column 3 Lines 46-49, wherein, the value of the mth strobe is interpreted as the most significant bit of an amplified frequency signal accumulated in a register).

8) Regarding claim 16:

Mueller teaches the method of claim 13 for re-sampling a plurality of N data sample inputs, wherein providing the timing signal comprises providing N timing signals in parallel (Paragraph 0025 Lines 1-4), and wherein re-sampling a data sample

comprises re-sampling N data samples in parallel, each at a time determined from one of the N timing signals (Paragraph 0024 Lines 4-7).

9) Regarding claim 17:

Mueller teaches a method for fractionally re-sampling a data sample, comprising:

inputting a symbol rate and a data strobe (Paragraph 0024 Lines 1-7).

As discussed in claim 10, Gardner et al. teaches:

measuring a difference between the data strobe and the symbol rate (Column 8 Lines 16-19 and Column 5 Lines 11-13, wherein, 'output error control signal' is interpreted as the difference between the data strobe and the symbol rate);

adjusting a next data strobe to match the symbol rate (Column 8 Lines 16-19, wherein, 'aligning' is interpreted as adjusting);

determining a timing signal based on the difference (Column 8 Lines 16-19, wherein, 'output error control signal' is interpreted as the timing signal); and

fractionally re-sampling a data sample at a time within a symbol period defined by the timing signal (Column 5 Lines 11-13).

10)Regarding claim 18:

Mueller discloses a circuit for re-sampling a data sample input comprising:

a numerically controlled oscillator NCO having an input coupled to the frequency adjustment output, and for outputting the data strobe and a timing signal (Paragraph 0025 Lines 1-4 and Page 4, Claim 1 Lines 3-4); and

a fractional interpolator having an inputs coupled to a data sample input, the data strobe, and the timing signal, for re-sampling the data sample input at a time within a symbol period defined by the timing signal (Paragraph 0024 Lines 4-7 and Page 4, Claim 1 Line 2).

Mueller does not disclose, a detector loop having an input coupled to an output of a symbol rate clock signal and to a data strobe, for determining a difference there between, and for providing a frequency adjustment output based on said difference. However, as discussed in claim 1 above, Gardner et al. discloses, a detector loop having an input coupled to an output of a symbol rate clock signal and to a data strobe, for determining a difference there between, and for providing a frequency adjustment output based on said difference (Column 2 Line 59 to Column 3 Line 5, Column 8 Lines 16-19, and Column 5 Lines 11-13, wherein, 'output error control signal' is interpreted as the difference between the symbol rate clock signal and the data strobe).

11)Regarding claim 19:

Mueller discloses the circuit of claim 18 for re-sampling a plurality of N data sample inputs in parallel, wherein the NCO outputs a plurality of N timing signals in parallel (Paragraph 0025 Lines 1-4) and the fractional interpolator has as inputs N data inputs in parallel and the N timing signals in parallel, and re-samples each of the N data samples at a time defined by one of the N timing signals (Paragraph 0024 Lines 4-7).

6. Claims 2, 3, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller (US Pub 2003/0204542) and Gardner et al. (US 5,805,619), and further in view of Boerstler (US 6,353,369).

1) Regarding claim 2:

Mueller or Gardner et al. do not disclose, wherein the oscillator comprises a plurality of N amplifiers each defining a different gain. However, Boerstler discloses, wherein the oscillator comprises a plurality of N amplifiers each defining a different gain (Column 2 Lines 51-56, wherein, the integer seven is interpreted as N).

It is fundamental that a NCO comprises a plurality of N amplifiers each defining a different gain. Different amplifier gains allow for the production of various voltage levels at the amplifiers outputs, i.e., allow for the production of various voltage levels to be coupled to the oscillator. Various voltage levels coupled to the oscillator, in turn, allow for the production of greater number of possible NCO output states. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the NCO of Mueller and Gardner et al. a plurality of N amplifiers each defining a different gain, as Boerstler teaches, in order to increase the number of possible NCO output states.

Regarding; wherein the strobe comprises a most significant bit selected from an output of one of the amplifiers, and wherein N is an integer greater than one, Gardner et al. further discloses, wherein the strobe comprises a most significant bit selected from an output of one of the amplifiers, and wherein N is an integer greater than one (Column

3 Lines 46-49, wherein, the value of the mth strobe is interpreted as the most significant bit selected from an output of one of the amplifiers).

2) Regarding claim 3:

As discussed in claim 2, Boerstler discloses wherein each of the N timing signals are coupled to an output of an associated amplifier (Column 2 Lines 51-56, wherein, each of the outputs of the inverter amplifiers is interpreted as each of the N timing signals).

Regarding, each timing signal except that coupled to a highest gain amplifier is independent of a most significant bit output from said associated amplifier. As discussed in claim 2, Gardner et al. discloses, each timing signal except that coupled to a highest gain amplifier is independent of a most significant bit output from said associated amplifier (Column 3 Lines 46-49, wherein, the value of the mth strobe is interpreted as the signal that is coupled to a highest gain amplifier and is not independent of a most significant bit output from said associated amplifier).

3) Regarding claim 12:

Mueller or Gardner et al. do not disclose, wherein N is greater than one, and the N data outputs are output at a rate at least equal to a symbol rate determined by the symbol rate clock, however, as discussed in claim 2, Boerstler discloses, wherein N is greater than one, and the N data outputs are output at a rate at least equal to a symbol rate determined by the symbol rate clock (Column 2 Lines 51-56, wherein, the integer seven is interpreted as the number of outputs, N, that is greater than one).

7. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller (US Pub 2003/0204542) and Gardner et al. (US 5,805,619), and further in view of Eory (US 5,832,043).

1) Regarding claim 4: (claim as interpreted by examiner)

Gardner et al. further discloses, wherein the fractional interpolator filter comprises:

a shift register having parallel inputs coupled to the N data inputs and to the strobe (Column 24 Lines 54-55).

Mueller or Gardner et al. do not disclose, N error-formatters each having an input coupled to a timing signal, for each outputting a first error value that depends at least in part from a most significant bit (MSB) defined by the timing signal and for outputting a second error value that depends at least in part from at least one other bit defined by the timing signal that is not the MSB. However, Eory discloses, N error-formatters each having an input coupled to a timing signal, for each outputting a first error value that depends at least in part from a most significant bit (MSB) defined by the timing signal and for outputting a second error value that depends at least in part from at least one other bit defined by the timing signal that is not the MSB (Column 6 Lines 1-12).

It is desirable to have N error-formatters (N bit splitters) in the circuit of Mueller and Gardner et al. A bit splitter allows for the separation and distinction of most significant bits from least significant ones. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include N error-

formatters (N bit splitters) in the circuit of Mueller and Gardner et al., as Eory discloses, in order to distinguish between most significant bits and least significant bits.

2) Regarding claim 5: (claim as interpreted by examiner)

Mueller further discloses, wherein the fractional interpolator filter further comprises:

N sub-blocks each having an input coupled to an output of the shift register and an input coupled to an output of an error-formatter (Paragraph 0027 Lines 1-3).

Regarding, coupled to an output of an error-formatter (bit splitter), as discussed in claim 4 above, Eory discloses and error-formatter (Column 6 Lines 1-2).

3) Regarding claim 6: (claim as interpreted by examiner)

Mueller further discloses, wherein the sub-blocks are of the type Farrow sub-blocks, linear interpolators, or polynomial interpolators (Paragraph 0032 Lines 1-4).

8. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller (US Pub 2003/0204542) in view of Harnden et al. (US Pub 2003/0069009).

1) Regarding claim 20:

Mueller discloses a circuit for interpolating a plurality of data points from a plurality of data samples comprising:

a fractional interpolator having an input coupled to the input streams for interpolating at least one interpolated data point from the data samples input along each of the N input streams, and N parallel outputs for outputting in parallel the interpolated data points (Paragraph 0024 Lines 4-7 and Page 4, Claim 1 Line 2); and

a numerically controlled oscillator NCO having an output coupled to an input of the fractional interpolator for providing timing signals for each of the interpolated data points (Paragraph 0025 Lines 1-4 and Page 4, Claim 1 Lines 3-4);

wherein the interpolated data points exhibit an output rate of 1/T that is cyclically independent of the sample rate $1/T_s$ (Paragraph 0024 Lines 1-7, wherein, 'F_c' is interpreted to correspond to $1/T_s$ and 'F_i' to correspond to 1/T).

Mueller does not disclose means for separating a plurality of at least 2N input data samples into N parallel input streams, the 2N data samples defining a sample rate of $1/T_s$. However, Harnden et al. discloses means for separating a plurality of at least 2N input data samples into N parallel input streams, the 2N data samples defining a sample rate of $1/T_s$ (Paragraph 0041 Lines 1-6, wherein, 'm' interpreted to be 2N and 'n' is interpreted to be N).

It is clearly obvious to one skilled in the art that a complex signal must be reproduced at the receiver, using the I and Q components, before interpolation is to be performed on said signal. Reproducing the complex signal using a polyphase filter comprising 2N inputs and N outputs results in much lower delay and greater computational efficiency. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include means for separating a plurality of at least 2N input data samples into N parallel input streams, such as the polyphase filter disclosed by Harnden et al., in the circuit of Mueller, in order to result in an interpolation circuit with lower delay and greater computational efficiency.

2) Regarding claim 21:

Mueller discloses, wherein the NCO has an input coupled to an output of a timing source that is independent of a timing source used for the input data samples (Paragraph 0028 Lines 1-5).

Allowable Subject Matter

9. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to clearly teach or suggest an error detector sub-circuit comprising a first state machine, and a second and third state machines in parallel with an oscillator input coupled to an output of at least one of the second or third state machines.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bossmeyer et al. (US Pub 2004/0148319) discloses a method and an apparatus for converting a first digital signal having a first sample rate to a second digital signal having a second sample rate. Conversion is achieved using a fractional converter.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached Monday through Friday, 8:30am- 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi December 9, 2006

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER